Blakely, Sokoloff, Taylor & Zafman LLP   (408) 947-8200
Title: Method and Apparatus For Cache Replacement For A Multiple
Variable-Way Associative Cache
1st Named Inventor: Salvador Palanca
Application No.: 09/608,507   Docket No.: 42390P8918
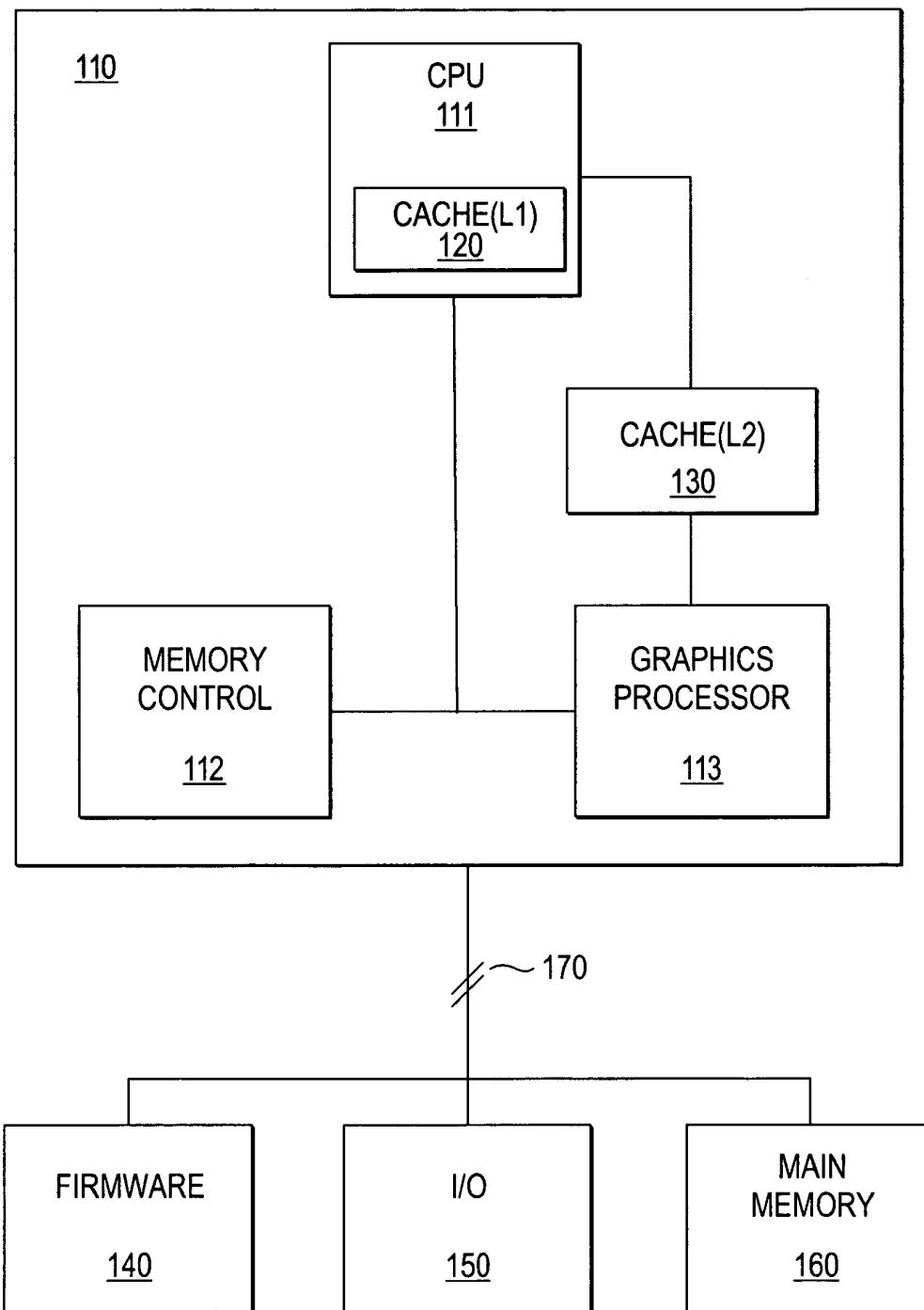Sheet: 1 of 8

100

FIG. 1

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Application No.: 09/608,507
Docket No.: 42390P8918
Sheet: 2 of 8

300

309   310

				311	312
0_A	1_A	0_B	1_B	C	D
2_A	3_A	2_B	3_B		
313		314		315	316
E		F		G	H
317		318		319	320
I		J		K	L
321		322		323	324
M		N		O	P

FIG. 2

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Application No.: 09/608,507
Sheet: 3 of 8   Docket No.: 42390P8918

PSEUDO-LRU REPLACEMENT MECHANISM

ENTRY:

PSEUDO-LRU UPDATE BASED ON ENTRY HIT

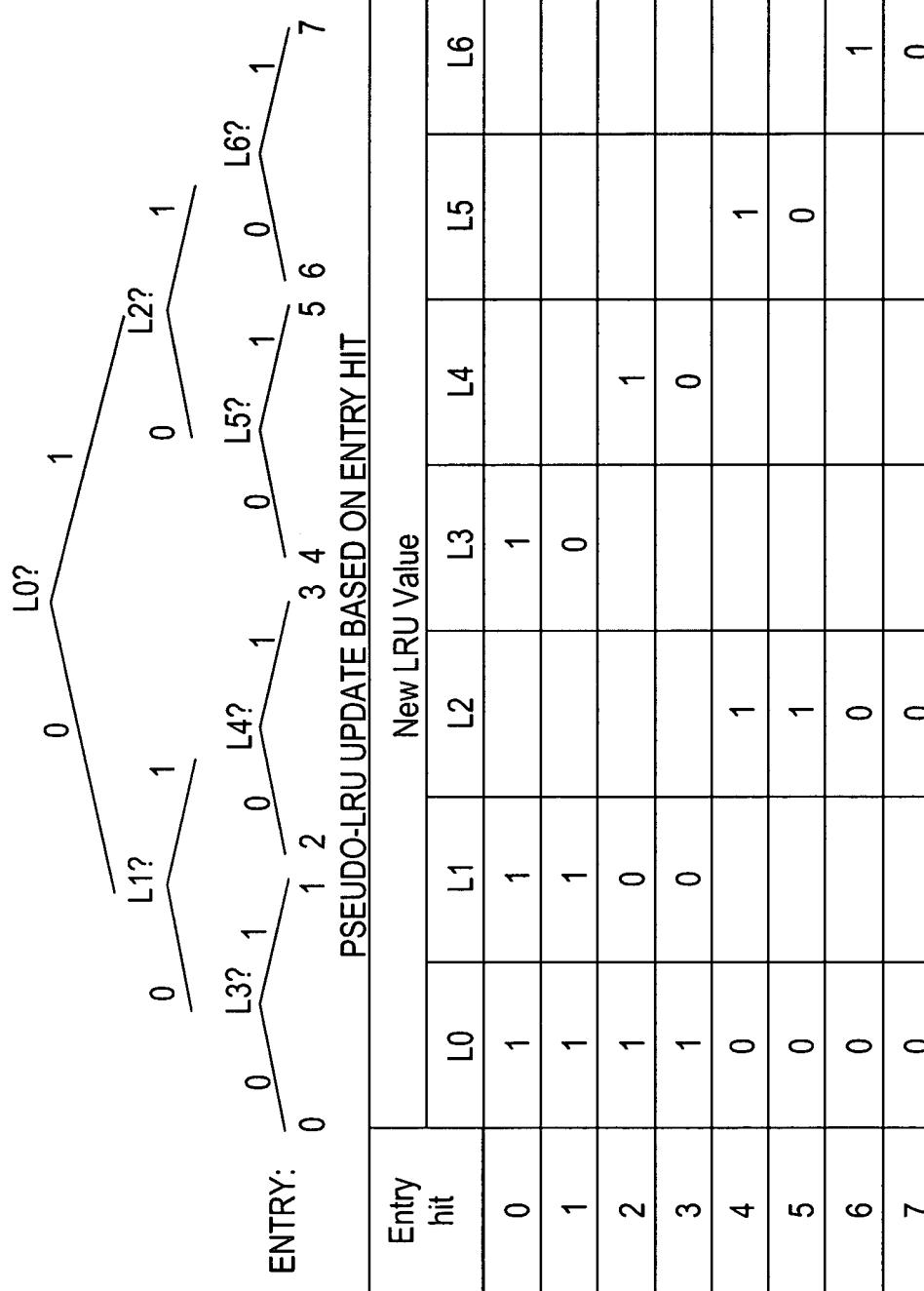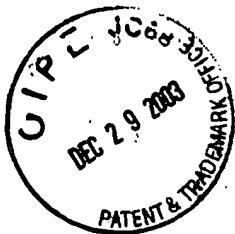| Entry hit	New LRU Value						
	L0	L1	L2	L3	L4	L5	L6
0	1	1		1			
1	1	1		0			
2	1	0			1		
3	1	0			0		
4	0		1			1	
5	0		1			0	
6	0		0				1
7	0		0				0

FIG. 3

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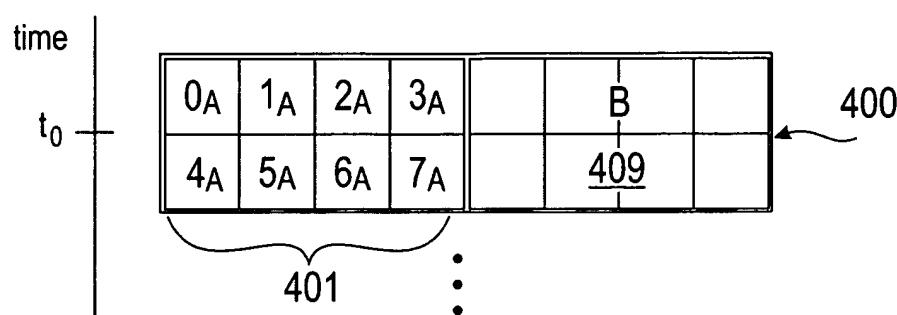Application No.: 09/608,507   Docket No.: 42390P8918
Sheet: 4 of 8

time

t₀

0ᴀ	1ᴀ	2ᴀ	3ᴀ		B	
4ᴀ	5ᴀ	6ᴀ	7ᴀ		409	

400

401

FIG. 4A

t₁

0ᴀ	1ᴀ	0ʙ	0ᴄ			
2ᴀ	3ᴀ	1ʙ	1ᴄ			

400

411   412   413   419

FIG. 4B

t₂

0ᴀ	1ᴀ	2ᴀ	0ʙ	C
3ᴀ	4ᴀ	5ᴀ	1ʙ	429

400

421   422

FIG. 4C

t₃

0ᴀ	1ᴀ	2ᴀ	3ᴀ	B
4ᴀ	5ᴀ	6ᴀ	7ᴀ	439

400

431

FIG. 4D

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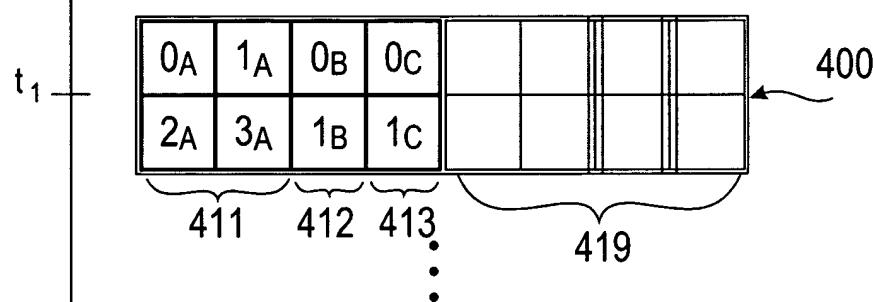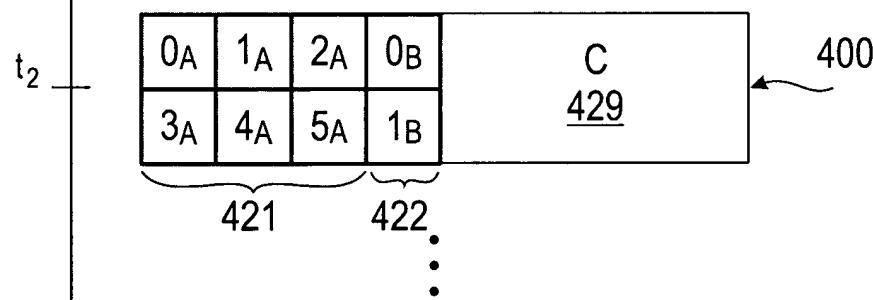Application No.: 09/608,507
Sheet: 5 of 8

Docket No.: 42390P8918

Color/Z

Texture

Not cached

CPU

ENTRY:

L0L1?

00   01   10

L3?   L4?   L5?   L6?

0   1   0   1   0   1   0   1

0   1   2   3   4   5

FIG. 5

500

Set 0

0
1

510

Set 1

0
1

520

Set 0

| 0 |

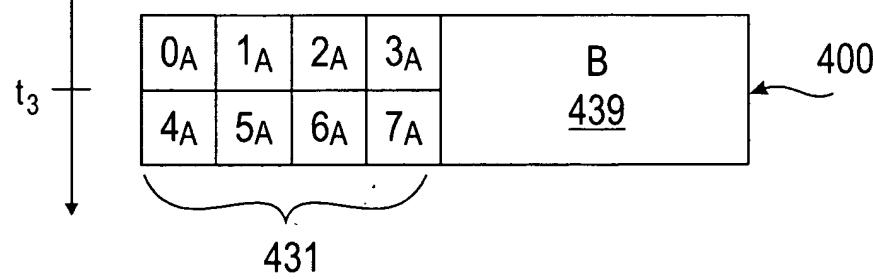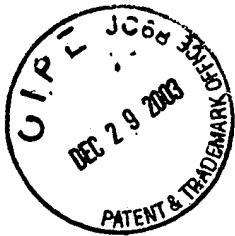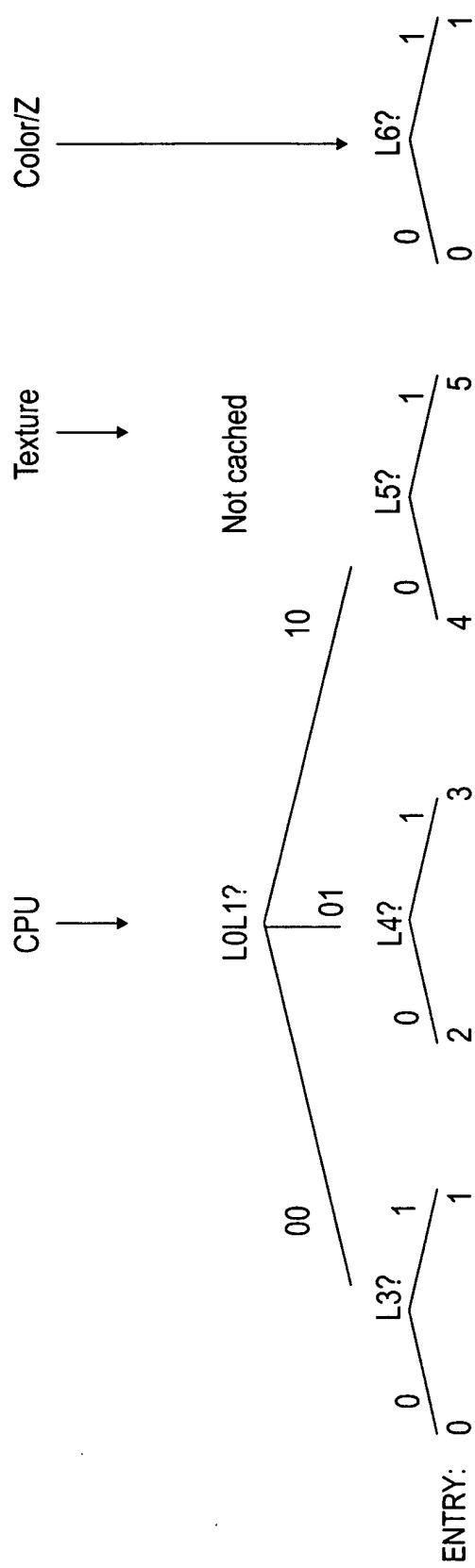511

Set 1

| 0 |

521

Set 2

| 0 |

512

Set 3

| 0 |

522

FIG. 6

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1st Named Inventor. Salvador Palanca
Application No.: 09/608,507
Sheet: 7 of 8   Docket No.: 42390P8918

START
600

Take an N-way set associative cache array, where N=(2 to the power M).
The cache has L sets, where L=(2 to the power K).
The cache line size is H bytes, where H=(2 to the power J).
The cache is byte addressable, and the physical address, i.e., PA, is Z bits.

610

PA[Z:0] = tag + set + byte offset = [Z:J+K]+[J+K-1,J]+[J-1,0]

620

Physical address for single access cache

Apply set subdivision to implement cache sharing

625

Support two simultaneous accesses in cache sharing mode with configuration 1/2-1/2.
The two request types supported are A and B; i.e., CPU and color/Z, with half a cache for each.
CPU and color/Z are allocated L/2 sets each.
Number of ways allocated to each request type remains constant; i.e., N-ways.

630

Request B: i.e., color/Z is allocated L/2 sets and N ways:
PA[Z:0] = tag + set + byte offset = [Z:J+K-1]+[J+K-2,J]+[J-1,0]

640

Physical address for cache size allocated to request type B

Convert to direct-mapped cache for request type B

645

Cache for request type B changed from N ways to direct-mapped:
PA[Z:0] tag + set + byte offset = [Z:J+K-1+M]+[J+K-2+M,J]+[J-1,0]

650

Physical address for direct-mapped cache for request type B

END
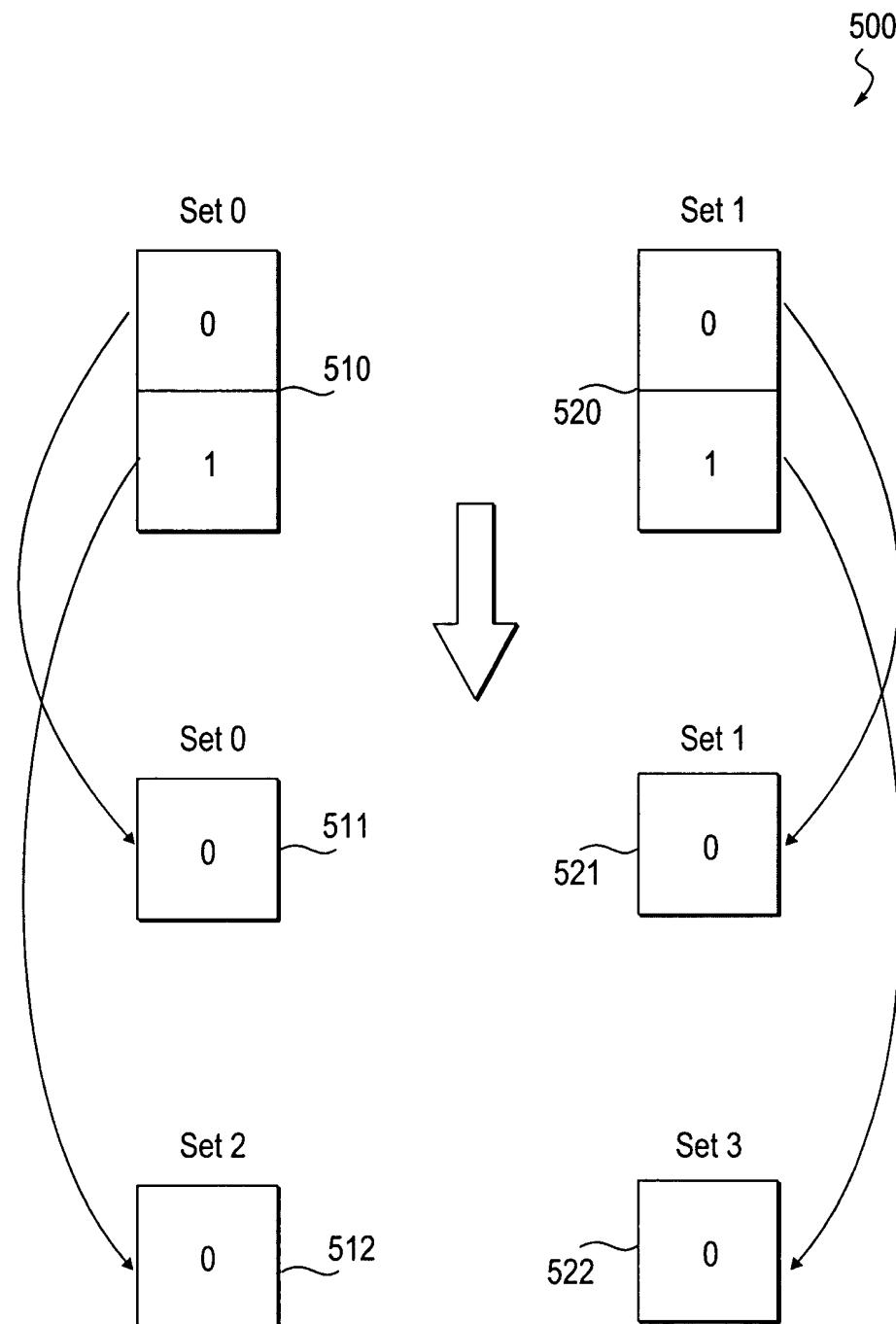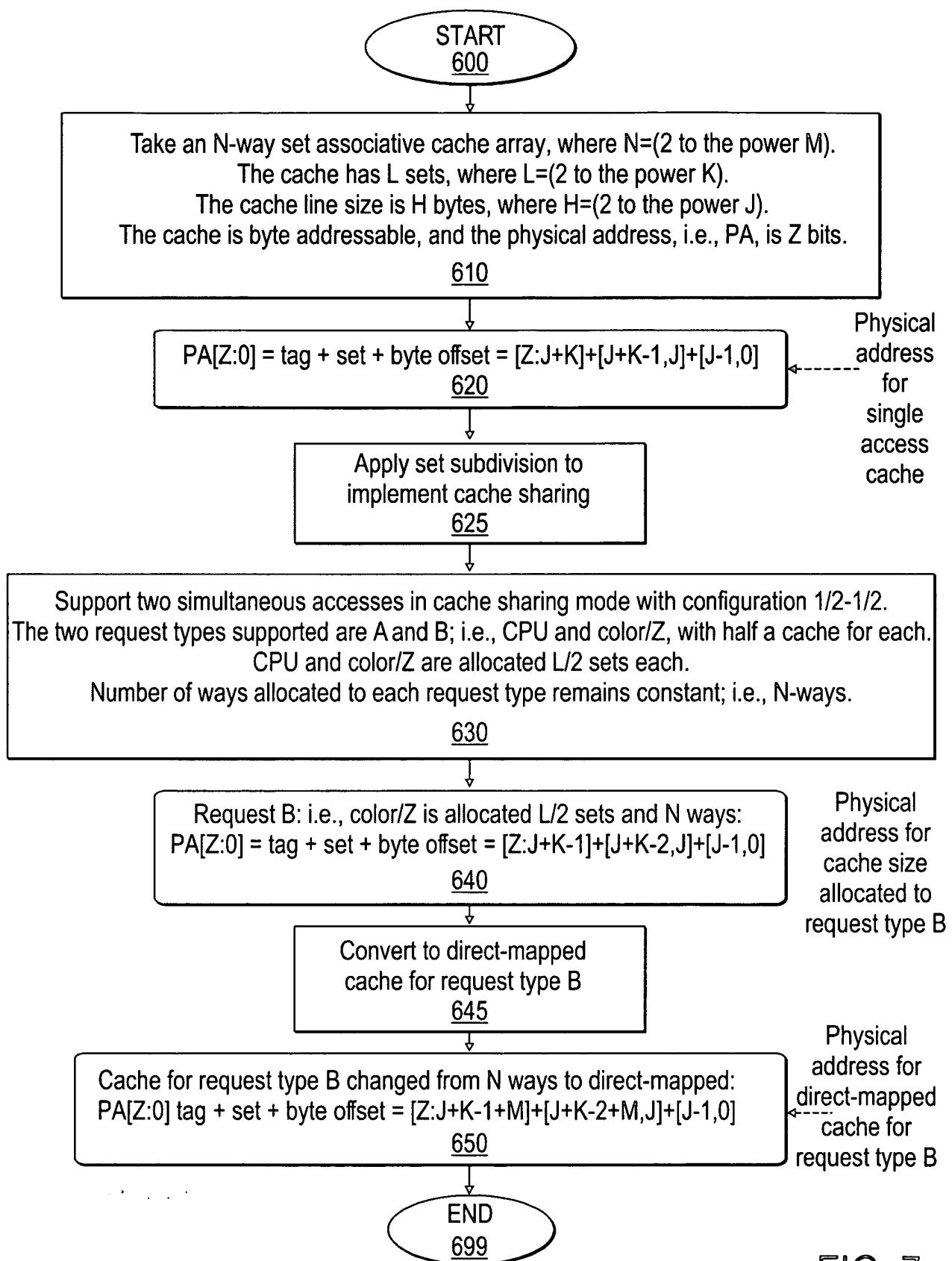699

FIG. 7

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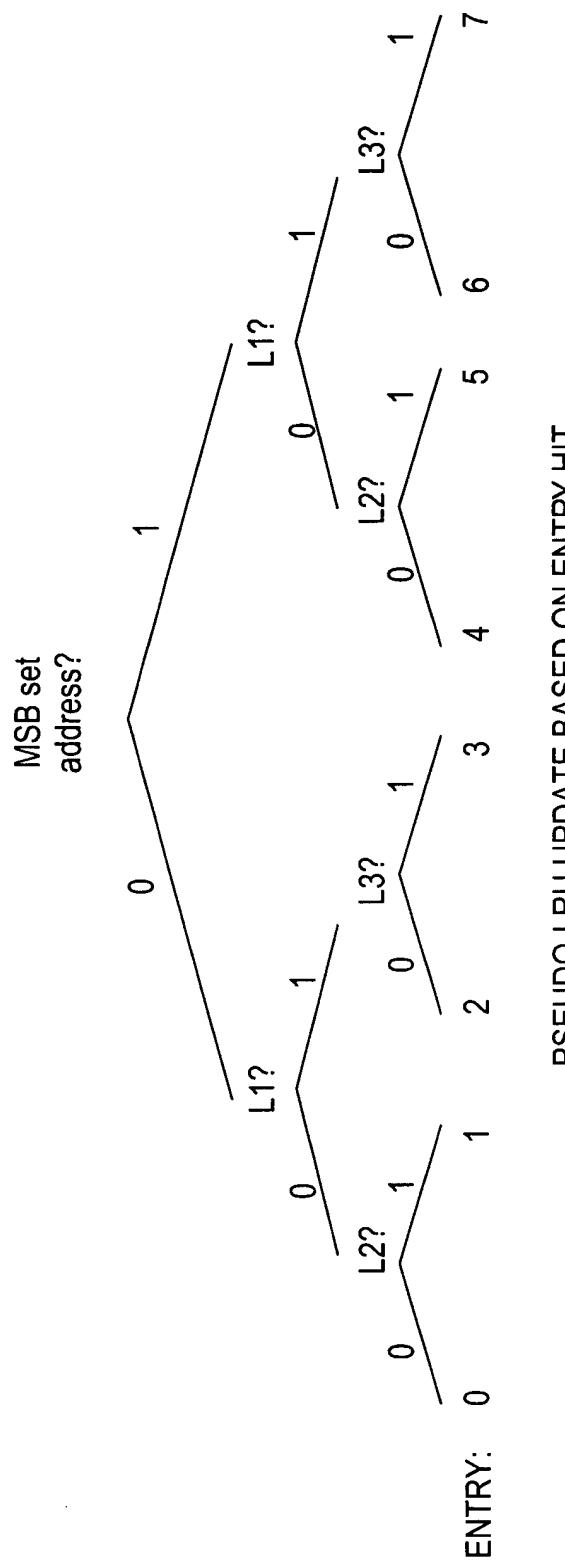Variable-Way Associative Cache
1st Named Inventor: Salvador Palanca
Application No.: 09/608,507
Sheet: 8 of 8   Docket No.: 42390P8918

FIG. 8

PSEUDO-LRU UPDATE BASED ON ENTRY HIT

Entry hit	New LRU value			
	MSB	L1	L2	L3
0	1	1	1	
1	1	1	0	
2	1	0		1
3	1	0		0
4	0	1	1	
5	0	1	0	
6	0	0		1
7	0	0		0